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November 23, 2005**from JOHN D. REED**

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To: Examiner Marcos D. Pizarro Crespo
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In re the application of

Serial No. : 10/729,859
Filed : December 5, 2003
For : MAGNETIC FIELD EFFECT TRANSISTOR, LATCH AND
METHOD
Group Art Unit : 2814
Examiner : Marcos D Pizarro Crespo
Attorney Docket : NAY 0001 PA/31558.2

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RECEIVED
CENTRAL FAX CENTER

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of)

Serial No.: 10/729,859)

Group Art Unit: 2814

Filed: December 5, 2003)

Examiner: Marcos D Pizarro Crespo

For: MAGNETIC FIELD EFFECT
TRANSISTOR, LATCH AND
METHOD)Attorney Docket:
NAY 0001 PA/31558.2MAIL STOP AMENDMENT
Commissioner of Patents and Trademarks
Washington, D.C. 20231
U.S.A.

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John Dinsmore

46,406
Reg. No.RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Dear Sir:

REMARKS

This responds to the Election/Restriction Requirement mailed as a second Office

Action on August 23, 2005.

Claims 1, 3-9 and 11-14 are pending.

In this second Office Action, the Examiner asserts for the first time that the
application is directed to multiple inventions, namely"Invention" I. Claims 1, 3, 4, 9, 11, 12 and 13, drawn to a semiconductor device,
classified in class 257, subclass 421 and"Invention" II. Claims 5 to 8, drawn to a method of using a semiconductor device,
classified in class 324, subclass 200

and that restriction is required.